

In the claims:

Please amend claims 15 and 27.

1 1. (Previously Presented) A system comprising:
2 a direct memory access (DMA) controller; and
3 an input/output (I/O) device coupled to the DMA controller, wherein the DMA
4 controller terminates a DMA transfer before a terminal count is reached upon receiving
5 an early termination request signal from the I/O device.

1 2. (Previously Presented) The system of claim 1 wherein the DMA controller re-
2 executes a DMA transfer with the I/O device upon receiving a retransmit request signal
3 from the I/O device.

1 3-5. Cancelled

1 6. (Previously Presented) The system of claim 1 further comprising:
2 a system interconnect coupled to the I/O device and the DMA controller;
3 a central processing unit (CPU) coupled to the system interconnect; and
4 a memory device coupled to the system interconnect.

1 7-11. Cancelled

1 12. (Previously Presented) A system comprising:
2 a direct memory access (DMA) controller; and
3 an input/output (I/O) device coupled to the DMA controller, wherein the DMA
4 controller re-executes a DMA transfer with the I/O device upon receiving a retransmit
5 request signal from the I/O device.

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1 13. (Previously Presented) A method comprising:
2 transferring data between a first device and a second device under control of a
3 direct memory access (DMA) controller;
4 receiving a request signal at the DMA controller from the first device indicating a
5 request by the first device to re-transmit the data between the first device and the second
6 device;
7 transmitting an acknowledge signal from the DMA controller to the first device;
8 and
9 re-transferring the data between the first device and the second device.

1 14. (Original) The method of claim 13 further comprising reloading configuration
2 registers within the DMA controller prior to transmitting the acknowledge signal to the
3 first device.

1 15. (Previously Presented) A method comprising:
2 transferring data between a first device and a second device under control of a
3 direct memory access (DMA) controller;
4 receiving a request signal at the DMA controller from the first device indicating a
5 request by the first device to ~~re-transmit~~ terminate the transfer of data between the first
6 device and the second device;
7 transmitting an acknowledge signal from the DMA controller to the first device;
8 and
9 terminating the transfer of data between the first device and the second device.

1 16. (Original) The method of claim 13 further comprising clearing a counter within
2 the DMA controller prior to transmitting the acknowledge signal to the first device.

1 17-20. Cancelled

1 21. (Previously Presented) The method of claim 15 further comprising:
2 receiving a second request signal at the DMA controller from the first device
3 indicating a request by the first device to re-transmit the data between the first device and
4 the second device;
5 transmitting a second acknowledge signal from the DMA controller to the first
6 device; and
7 re-transferring the data between the first device and the second device according
8 to the first set of commands.

1 22. (Previously Presented) The method of claim 15 further comprising:
2 receiving a second request signal at the DMA controller from the first device
3 indicating a request by the first device to re-transmit the data between the first device and
4 the second device;
5 transmitting a second acknowledge signal from the DMA controller to the first
6 device; and
7 terminating the transfer of data between the first device and the second device.

1 23. (Original) The method of claim 22 further comprising:

2 reducing a transfer count within the descriptor table after terminating the transfer;
3 and
4 retrieving a second set of commands from the descriptor table.

1 24. (Previously Presented) The system of claim 1 wherein the DMA controller
2 comprises a first channel coupled to the I/O device to facilitate the transfer of data.

C/ 1 25. (Previously Presented) The system of claim 24 wherein the DMA controller
2 further comprises a register, coupled to the channel, to store configuration data.

1 26. (Previously Presented) The system of claim 25 wherein the DMA controller
2 further comprises error checking logic.

1 27. (Currently Amended) The system of claim 24 wherein the channel comprises
2 control logic to control the transfer of data process within the first channel.

1 28. (Previously Presented) The system of claim 24 wherein the channel further
2 comprises descriptor logic to control the transfer of data in a descriptor mode.

1 29. (Previously Presented) The system of claim 12 wherein the DMA controller
2 comprises a first channel coupled to the I/O device to facilitate data transfers.

1 30. (Previously Presented) The system of claim 29 wherein the DMA controller
2 further comprises a register, coupled to the channel, to store configuration data.

1 31. (Previously Presented) The system of claim 30 wherein the DMA controller
2 further comprises error checking logic.

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- 1 32. (Previously Presented) The system of claim 29 wherein the channel comprises
 - 2 control logic to control the transfer of data.
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